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The EKV MOSFET Model for Circuit Simulation

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Motivation & Outline

- Motivation: analog and mixed analog-digital circuit design:
  - ✔ *need for a continuous, physics based MOSFET model*
  - ✔ *must represent weak and moderate inversion correctly*
  - ✔ *a model that allows designers to go from hand-calculation to full-circuit simulation (hierarchical structure)*
  - ✔ *need for meaningful statistical circuit simulation*
- Outline:
  - ✔ *the EKV MOSFET model structure*
  - ✔ *modelled effects and parameters*
  - ✔ *parameter extraction and results*
  - ✔ *model benchmarks and comparisons*
  - ✔ *outlook on future developments*

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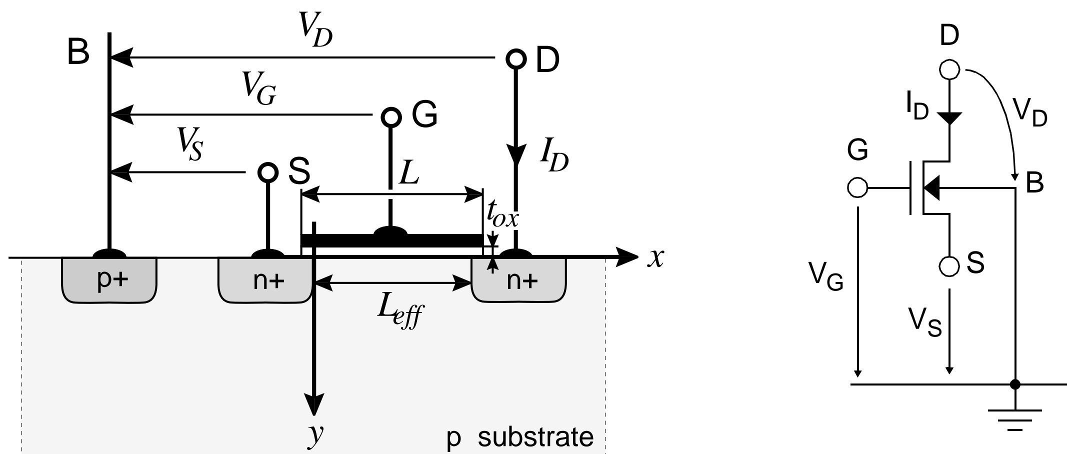
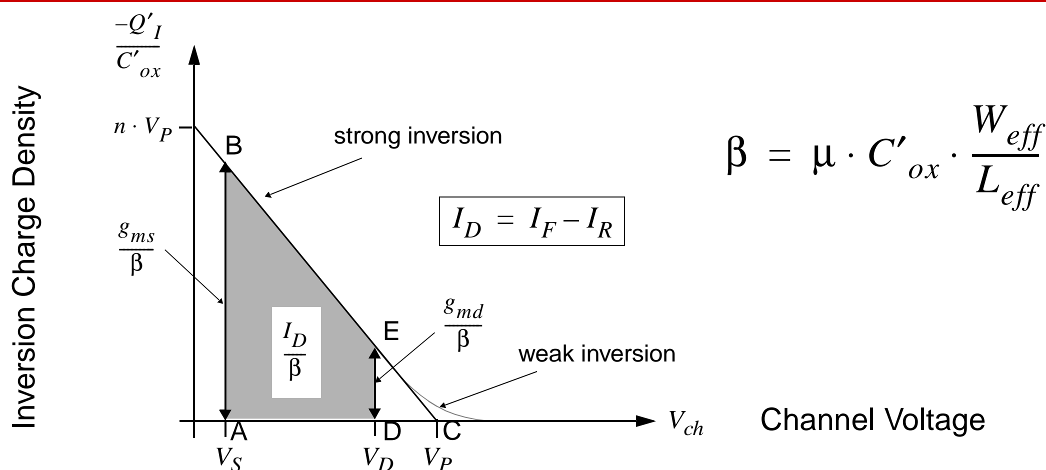
Model Structure (1/4) : Bulk Reference



- Bulk-reference, symmetric model structure.
- Drain current expression including drift and diffusion:

$$I_D = W \cdot \mu \cdot (-Q'_I) \cdot \frac{dV_{ch}}{dx} \tag{1}$$

Model Structure (2/4) : Drain Current



$$\beta = \mu \cdot C'_{ox} \cdot \frac{W_{eff}}{L_{eff}}$$

$$I_D = I_F - I_R$$

- Integration of Q'_I from source to drain:

$$I_D = \beta \int_{V_S}^{V_D} \left(\frac{-Q'_I}{C'_{ox}}\right) \cdot dV_{ch} = \underbrace{\beta \int_{V_S}^{\infty} \left(\frac{-Q'_I}{C'_{ox}}\right) \cdot dV_{ch}}_{I_F(V_P - V_S)} - \underbrace{\beta \int_{\infty}^{V_D} \left(\frac{-Q'_I}{C'_{ox}}\right) \cdot dV_{ch}}_{I_F(V_P - V_D)} \tag{2}$$

Model Structure (3/4) : Pinch-off Voltage

☞ Current normalization using the **Specific current** I_S:

$$I_D = I_F - I_R = I_S \cdot (i_f - i_r) = 2n\beta U_T^2 \cdot (i_f - i_r) \qquad (3)$$

☞ **Pinch-off voltage** V_P accounts for...

✔***threshold voltage*** V_{TO} *and* ***substrate effect*** $\gamma = (\sqrt{2q\varepsilon_s N_{sub}}) / C'_{ox}$

$$V_P = V_G - V_{TO} - \gamma \cdot \left[\sqrt{V_G - V_{TO} + \left(\sqrt{\Psi_0} + \frac{\gamma}{2}\right)^2} - \left(\sqrt{\Psi_0} + \frac{\gamma}{2}\right)\right] \qquad (4)$$

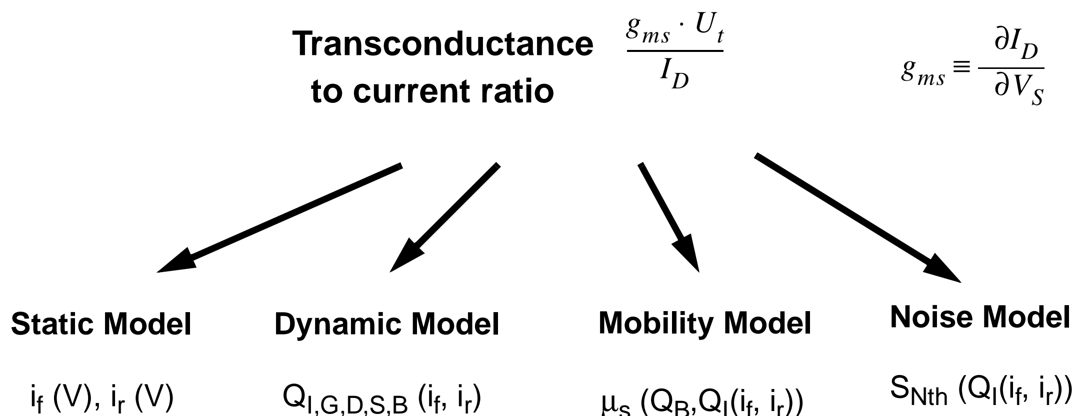
☞ **Slope factor** n:

$$n = \left[\frac{\partial V_P}{\partial V_G}\right]^{-1} = 1 + \frac{\gamma}{2\sqrt{\Psi_0 + V_P}} \qquad (5)$$

Model Structure (4/4) : Normalized G_{MS}/I_D Ratio

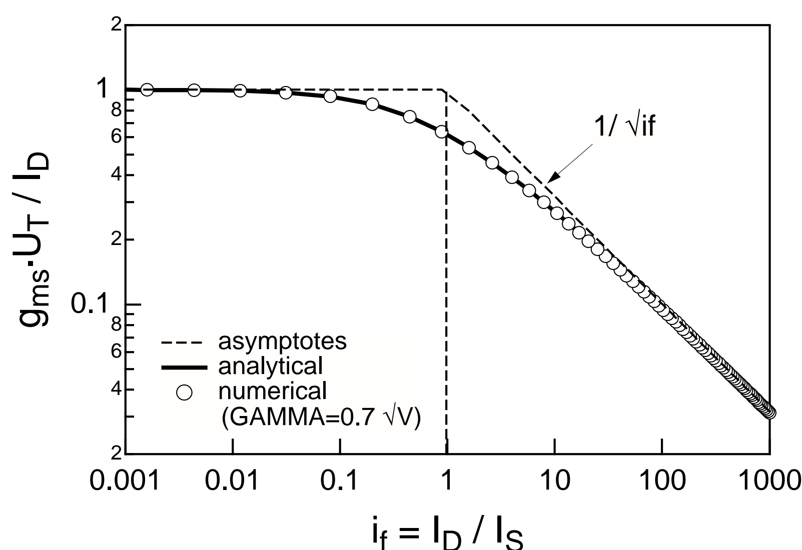
☞ Coherent model for static, dynamic and noise aspects.

✔*derived from the normalized transconductance-to-current ratio:*



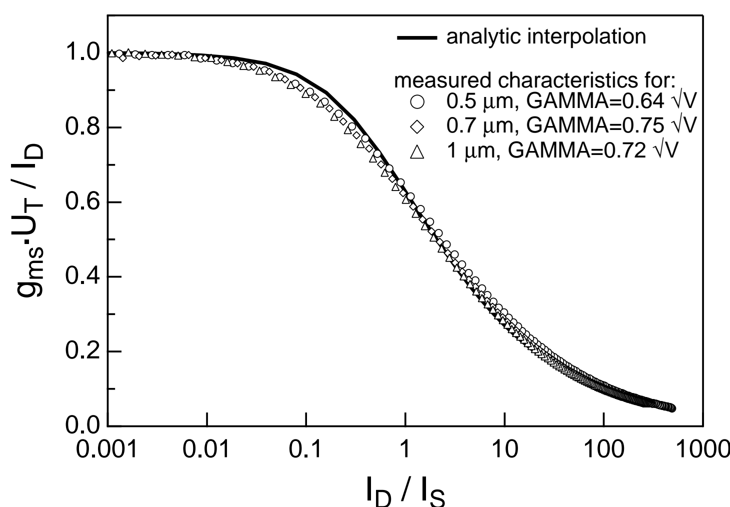
✔*common variable to the entire model: normalized currents i_f and i_r (forward and reverse)*

Normalized Transconductance vs. Current



- Normalized G_{MS}/I_D *vs.* I_D
  - ✔ *in saturation, from weak to strong inversion, compared to a numerical solution of the Poisson equation*

Normalized Transconductance vs. Current



- Three different CMOS technologies:
  - ✔ *universal behaviour, almost independent of technology*
  - ✔ *therefore, the EKV model is well adapted for a large range of technologies*
- Excellent match in the weak and moderate inversion regions.

Modelled Effects: Long-Channel

- Physics-based modelling of weak, moderate and strong inversion.
- Relation with geometrical and process variables as:
  - ✔ *oxide thickness, junction depth*
  - ✔ *effective channel length and width*
- Effects of substrate doping level, substrate effect.
- Vertical field dependent mobility.

Modelled Effects: Short-Channel

- Common short-channel effects:
  - ✔ *velocity saturation*
  - ✔ *channel length modulation (CLM)*
  - ✔ *two-dimensional bulk charge-sharing for short-and narrow-channel effects*
  - ✔ *reverse short-channel effect (RSCE)*
  - ✔ *substrate current effects on drain conductance*
- Short-distance matching for statistical circuit simulation.
  - ✔ *area- and bias-dependent device matching for:*
    - *threshold voltage*
    - *gain factor (mobility)*
    - *substrate effect*
  - ✔ *a unique feature which is commonly unavailable in other public-domain models!*

EKV v2.6: 18 Intrinsic Model Parameters

Purpose	NAME	DESCRIPTION	UNITS	EXAMPLE
Process parameters	COX	gate oxide capacitance per unit area	F/m^2	3.45E-3
	XJ	junction depth	m	0.15E-6
	DW	channel width correction	m	-0.05E-6
	DL	channel length correction	m	-0.1E-6
Doping & Mobility related parameters	VTO	long-channel threshold voltage	V	0.55
	GAMMA	body effect parameter	$\sqrt{V}$	0.7
	PHI	bulk Fermi potential (*2)	V	0.8
	KP	transconductance parameter	A/V^2	160E-6
	E0	vertical characteristic field for mobility reduction	V/m	80E6
	UCRIT	longitudinal critical field	V/m	4.0E6
Short- & narrow-channel effect parameters	LAMBDA	depletion length coefficient (channel length modulation)	-	0.3
	WETA	narrow-channel effect coefficient	-	0.1
	LETA	short-channel effect coefficient	-	0.3
	Q0	reverse short-channel effect peak charge density	$A \cdot s/m^2$	500E-6
	LK	reverse short-channel effect characteristic length	m	0.34E-6
Substrate current related parameters	IBA	first impact ionization coefficient	$1/m$	260E6
	IBB	second impact ionization coefficient	V/m	350E6
	IBN	saturation voltage factor for impact ionization	-	1.0

☞ Completed with 2 noise, 4 temperature and 3 matching parameters.

Statistical Circuit Simulation Including Matching

NAME	DESCRIPTION	UNITS	Example
AVTO	area related threshold voltage mismatch parameter	Vm	- DEV=15E-9
AKP	area related gain mismatch parameter	m	- DEV=25E-9
AGAMMA	area related body effect mismatch parameter	$\sqrt{V}m$	- DEV=10E-9

☞ Area related mismatch model (Pelgrom e.a.):

$$\mathrm{VTO}_a = \mathrm{VTO} + \frac{\mathrm{AVTO}}{\sqrt{W_{eff} \cdot L_{eff}}} \quad (6)$$

$$\mathrm{GAMMA}_a = \mathrm{GAMMA} + \frac{\mathrm{AGAMMA}}{\sqrt{W_{eff} \cdot L_{eff}}} \quad (7)$$

$$\mathrm{KP}_a = \mathrm{KP} \cdot \left(1 + \frac{\mathrm{AKP}}{\sqrt{W_{eff} \cdot L_{eff}}}\right) \quad (8)$$

✔ *during Monte-Carlo statistical circuit simulation, the parameters are individually varied for each matched transistor.*

☞ Leads to an important reduction of simulation effort!

✔ *no need to create individual parameter sets for each geometry*

Vertical Field Dependent Mobility

- Local effective field dependence on depletion and inversion charges:

$$E_{eff}(x) = \frac{Q'_B(x) + \eta \cdot Q'_I(x)}{\varepsilon_0 \varepsilon_{si}} \quad (9)$$

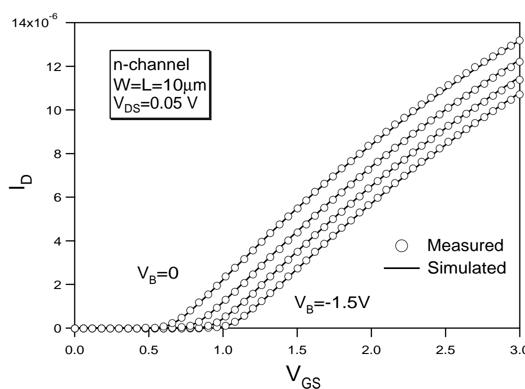
- Local mobility dependence on vertical field:

$$\mu(x) = \frac{\mu_0'}{1 + \frac{E_{eff}(x)}{E0}} \quad (10)$$

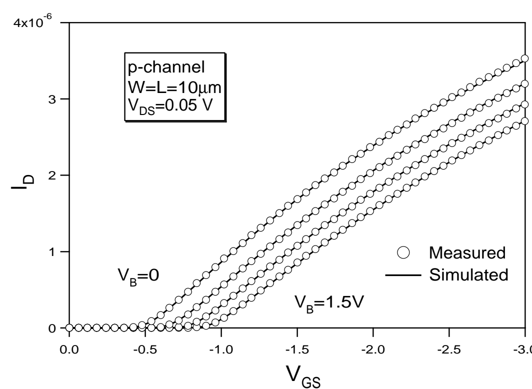
  - ✔ $\eta = 1/2$ *for n-channel,* $\eta = 1/3$ *for p-channel*
  - ✔ *the parameter E0 is the vertical critical field across the oxide*

- Local mobility expression is integrated along the channel.

Mobility Model (0.5um CMOS)



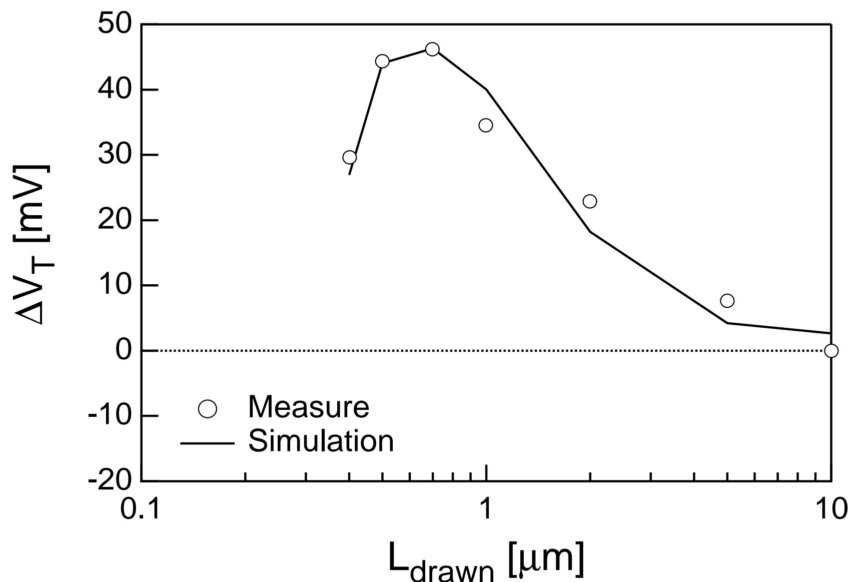
n-channel



p-channel

- Good behaviour for mobility reduction for n- and p-channels.
- Substrate effect is correctly accounted for.
- No back-bias dependence required!

Reverse Short-Channel Effect



- Measured/simulated change of threshold voltage vs. L_{drawn} (0.5µm n-channel).

Charge-Based Dynamic Model

- Integration of inversion charge density along the channel:

$$Q_I = W \cdot \int_0^L Q_I'(y) \cdot dy \tag{11}$$

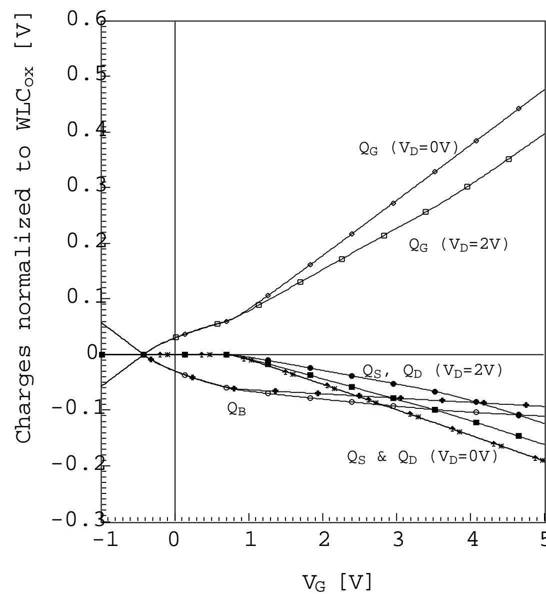
- Integration of Q_I is performed in terms of normalized current.
- Channel charge partitioning and gate charge:

$$Q_D = W \cdot \int_0^L \frac{y}{L} \cdot Q_I'(y) \cdot dy \qquad Q_S = Q_I - Q_D \qquad Q_G = -Q_I - Q_B \tag{12}$$

- Derivation of transcapacitances:

$$C_{XYZ} = \pm \frac{\partial}{\partial V_{YZ}}(Q_X(i_f, i_r)) \tag{13}$$

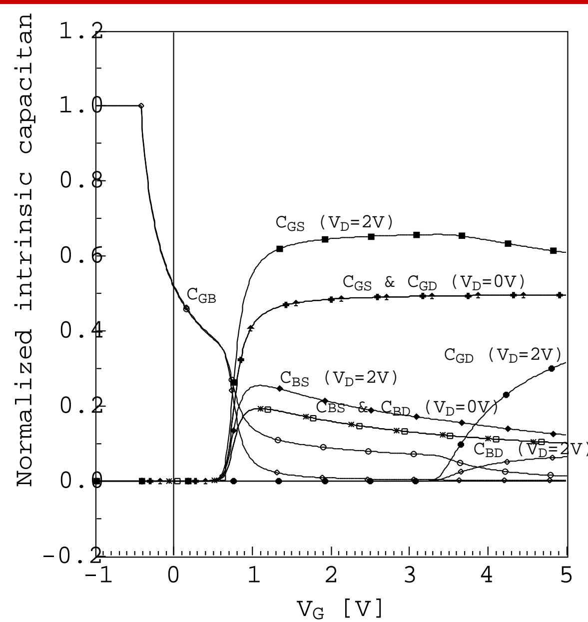
Charges vs. Gate Voltage



☞ Continuous node charges from weak to strong inversion.

✔*allows charge conservation in transient simulation*

Capacitances vs. Gate Voltage

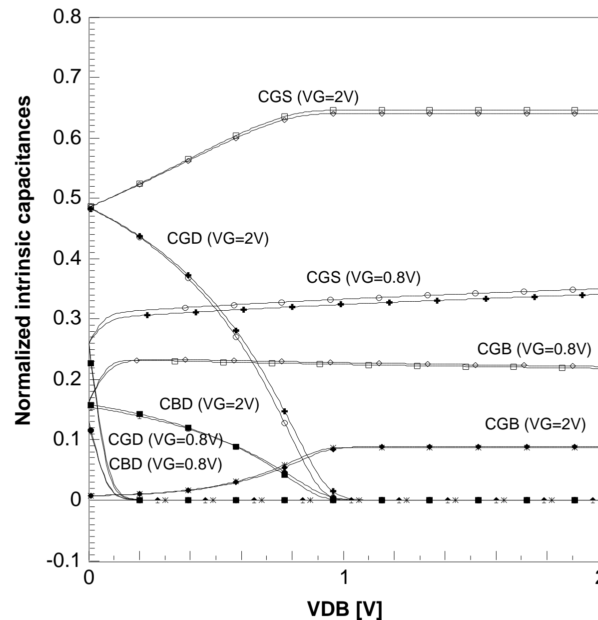


☞ Capacitances are valid in all operating regions:

✔*correct weak-to-strong inversion behaviour*

✔*continuous, and symmetric at V_{DS}=0*

Capacitances vs. Drain Voltage



- Smooth behaviour from conduction to saturation.
  - ✔ *comparison between new charge-based and former capacitances-only models*

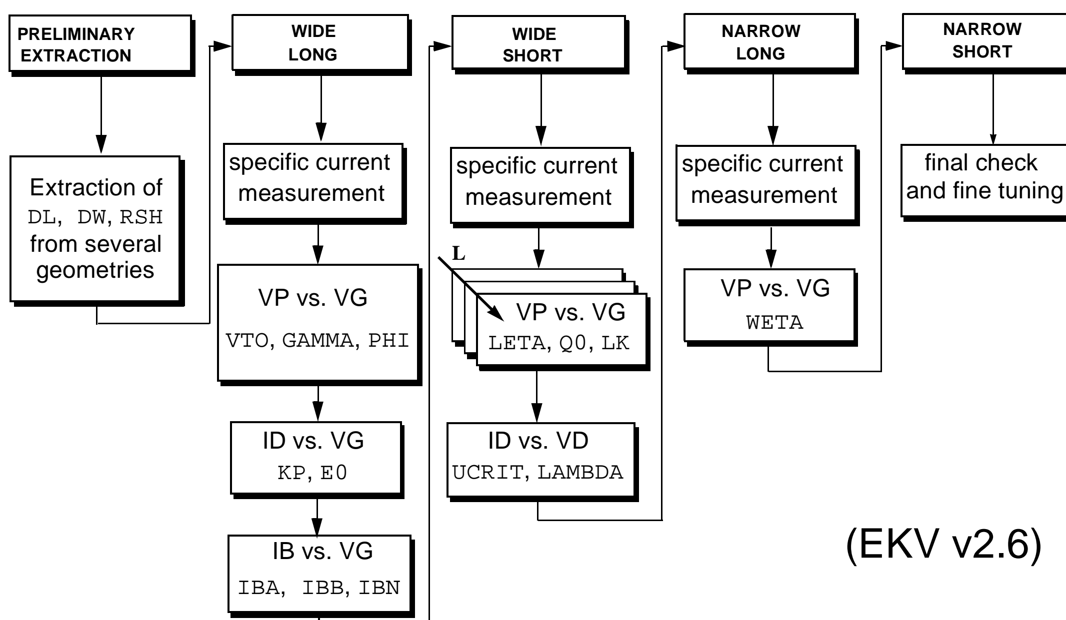
Dynamic Model - Summary

- Charge-based for charge conservation in transient simulation.
- Charges and transcapacitances are "smooth":
  - ✔ *valid from weak to strong inversion and from conduction to saturation*
- Symmetric operation in terms of V_D and V_S.
- Short-channel effects are included through the pinch-off voltage V_P (charge-sharing, RSCE).
- Extensions are under development:
  - ✔ *velocity saturation and space-charge effects on capacitances*
  - ✔ *bias dependent overlap capacitances*

Parameter Extraction Method

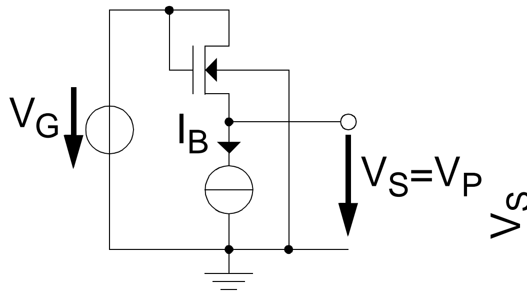
- Hierarchical structure allows separation of physical effects and parameters.
- Mixed direct extraction and local optimization is used.
- Dedicated parameter extraction method:
  - ✔ *based on pinch-off voltage measurement technique [1] to determine substrate effect, including for charge-sharing and RSCE.*
- Uses array of transistors in the W/L plane.
- Sequential task that can be automated.
  - ✔ *well suited for statistical purposes*

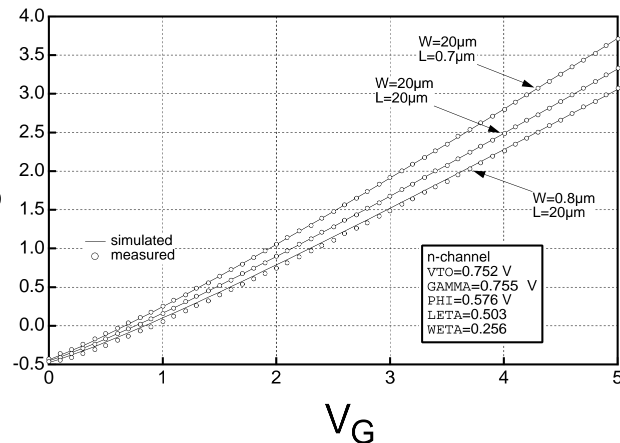
Parameter Extraction Sequence (DC)



- Extraction sequence using direct extraction and optimization.

Pinch-off Voltage Measurement Method

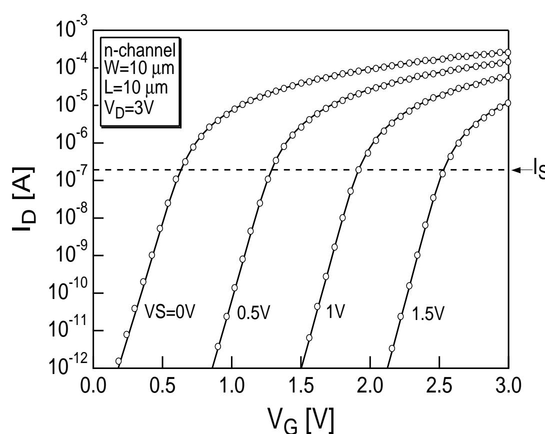


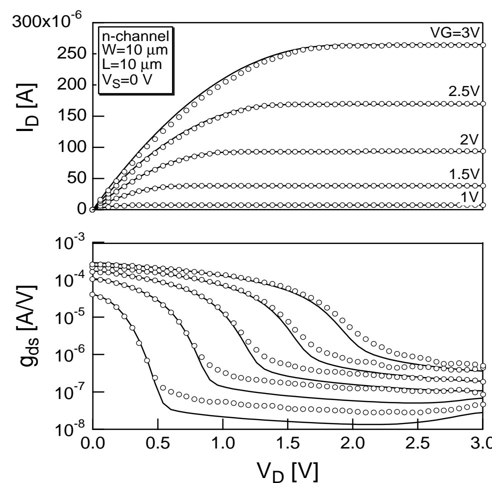


$$I_B \cong \frac{I_S}{2} = n \cdot \beta \cdot U_T^2$$

- Constant current bias for the V_P vs. V_G measurement.
  - ✔ *used for different channel lengths and widths*
- Direct parameter extraction for threshold voltage and substrate effect parameters.

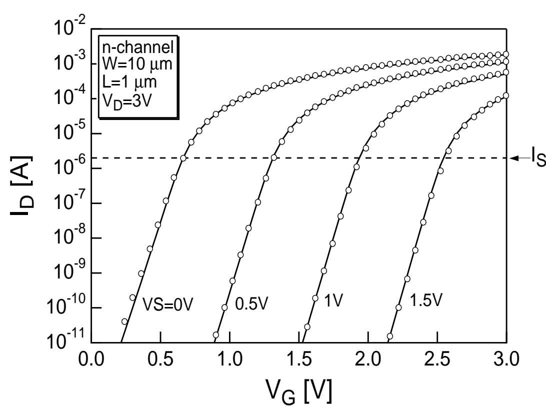
Submicron (0.5um) CMOS: Long-Channel Characteristics

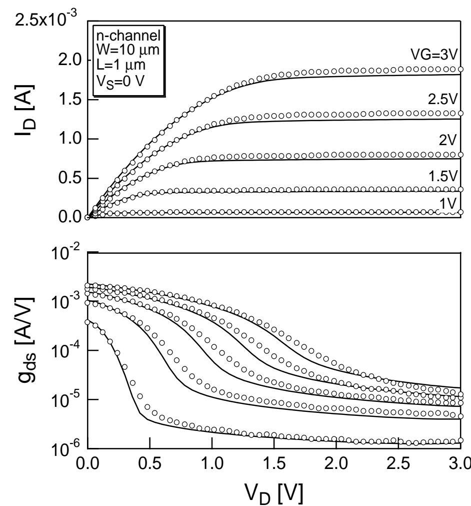




- Weak-to-strong inversion continuity.
- Accuracy of weak inversion slope and substrate effect.
  - ✔ *no additional parameters used for adapting weak inversion slope*

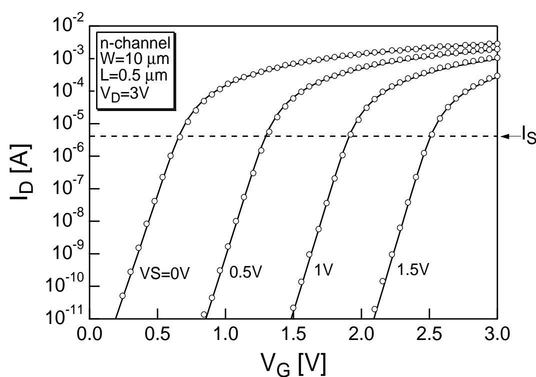
Submicron (0.5um) CMOS: Intermediate Channel-Length Characteristics

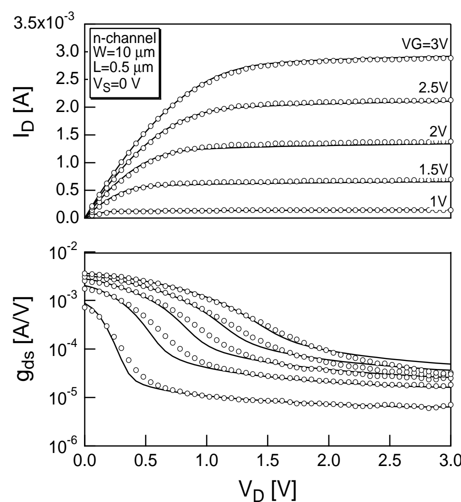




- Correct threshold voltage.
- Demonstrates good scaling behaviour.

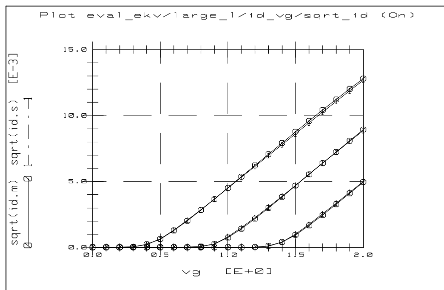
Submicron (0.5um) CMOS: Short-Channel Characteristics

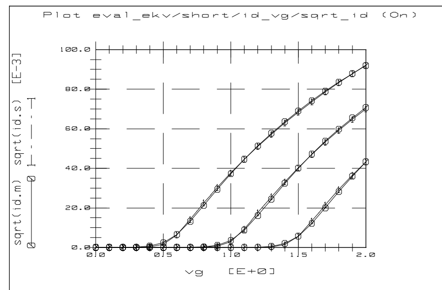


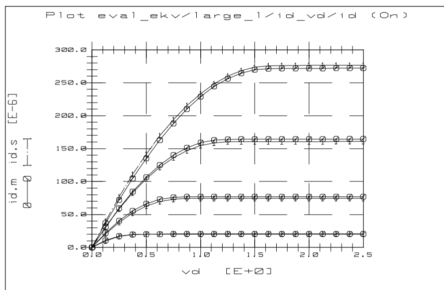


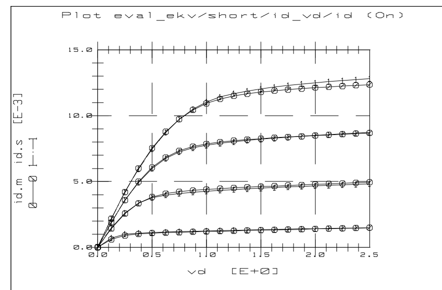
- Accurate output conductance for shortest channel transistor.
- Includes CLM, velocity saturation, substrate current.
- Single model card is used for all geometries.

Deep-Submicron (0.25um) CMOS







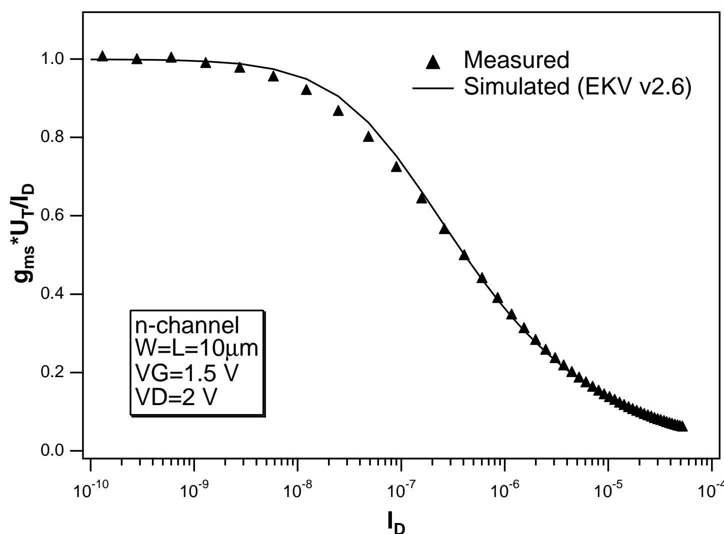


Long-channel

Short-channel (0.25um)

☞ EKV v2.6: results for 0.25um CMOS technology.

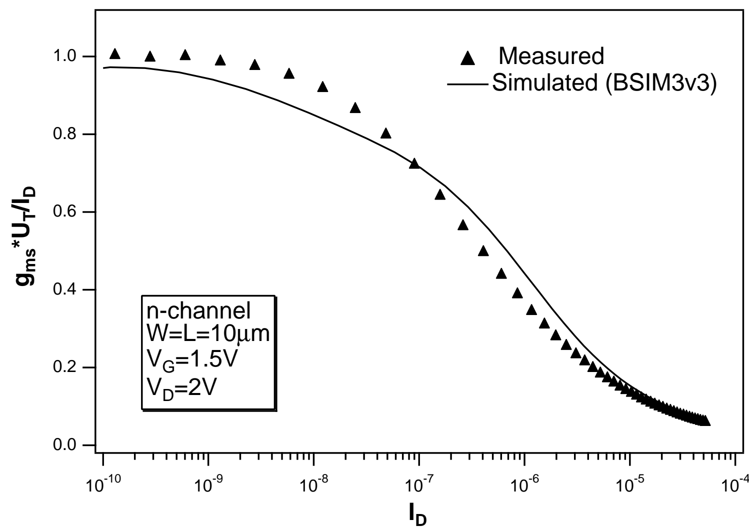
Benchmark: EKV $g_{ms} \cdot U_T/I_D$ vs. I_D



☞ EKV model exhibits qualitatively correct behaviour.

✔*no particular parameter adaptation is required*

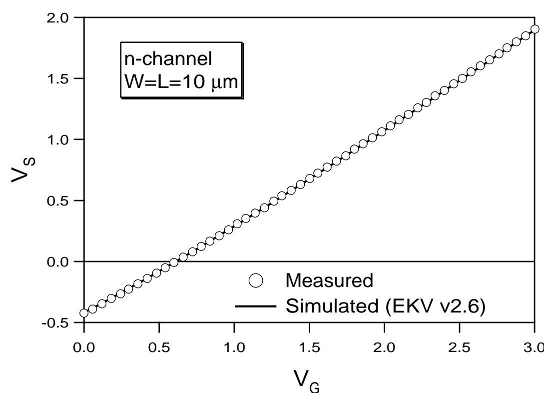
Benchmark: BSIM3v3 $g_{ms} \cdot U_T/I_D$ vs. I_D



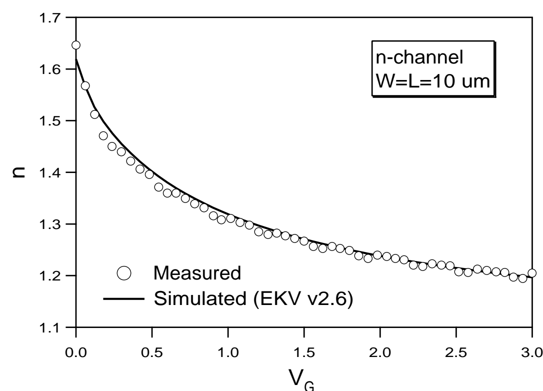
☞ BSIM3v3 exhibits qualitatively poor behaviour in weak and moderate inversion.

✔*parameter adaptation is required (*VOFF, NFACT*)*

Benchmark: Substrate Effect, EKV v2.6



V_P vs. V_G

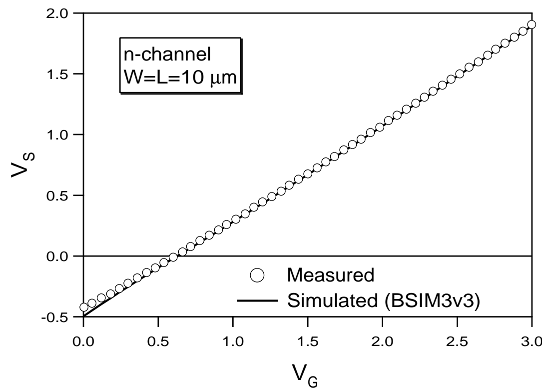


n vs. V_G

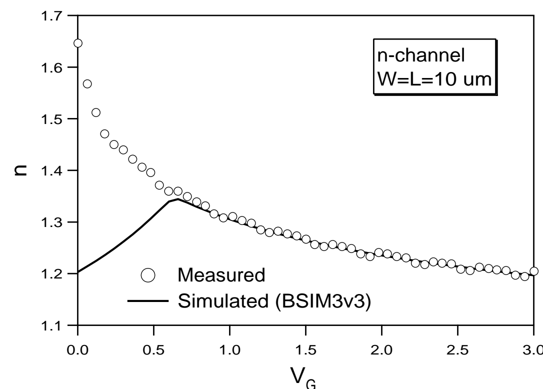
☞ Adequate behaviour over the whole bias range for EKV.

☞ Accurate prediction of slope factor n .

Benchmark: Substrate Effect, BSIM3v3



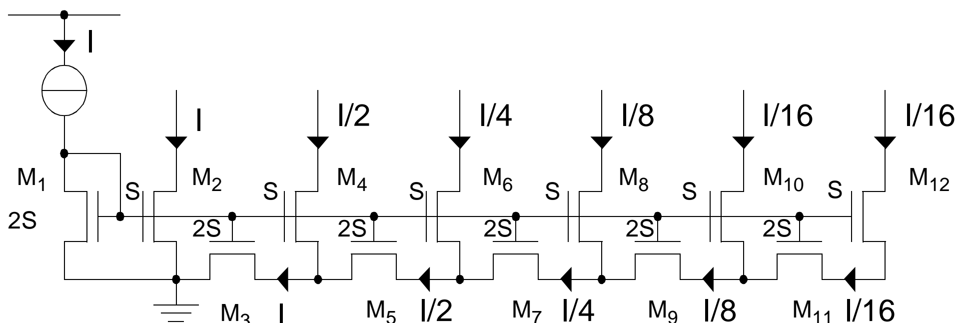
V_S vs. V_G



n vs. V_G

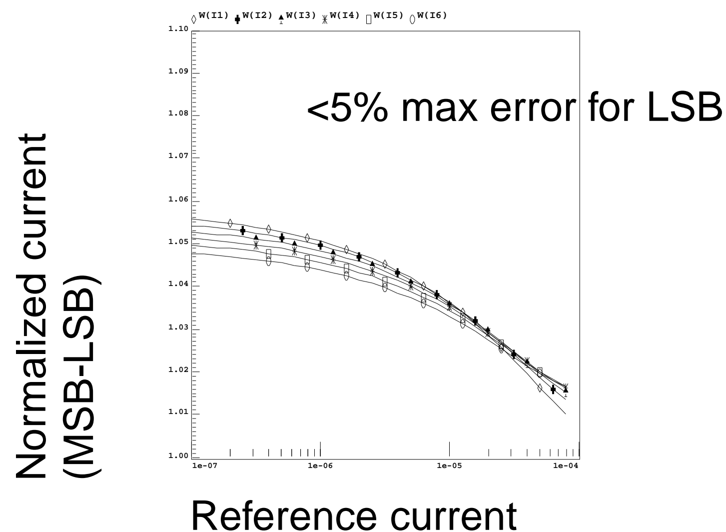
- Inadequate behaviour for negative V_{SB}
  - ✔ *possible origin of error: source reference!*

Benchmark: D/A Converter Circuit



- A typical current divider circuit used in D/A converters *[2]*.
  - ✔ *each stage divides the reference current by a factor of 2*
  - ✔ *principle of an R-2R ladder circuit*
- Expected behaviour: perfect current divider!
  - ✔ *ratio-based circuit technique (aspect ratios used: S, 2S)*

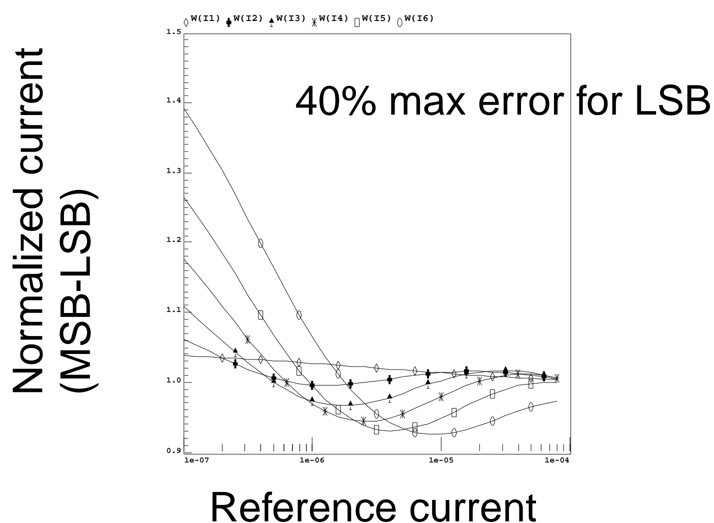
Benchmark: D/A Converter, EKV v2.6



☞ EKV model exhibits adequate ratio-based circuit behaviour

✔ *the converter works as should be expected according to circuit principle*

Benchmark: D/A Converter, BSIM3v3



☞ BSIM3v3 exhibits inadequate ratio-based circuit behaviour

✔ *a serious error in the circuit is predicted*

✔ *behaviour is unrelated to small geometry effects (long and wide MOS are used)*

Benchmarks - Summary

- A MOSFET model should provide “safe limits” for fundamental physical aspects
  - ✔*reliance on parameter extraction can be troublesome*
- Source-reference may result in non-physical behaviour.
- Physical limits are not guaranteed by the BSIM3v3 model in particular for the $g_{ms} \cdot U_t / I_D$ characteristic.
- Number of intrinsic model parameters used:
  - ✔*EKV v2.6: 18*
  - ✔*BSIM3v3: >65*
  - ✔*Philips MOS Model 9: >55*

EKV v2.6 Model Availability in Simulators

- Implementations available:
  - ✔*ELDO (Mentor Graphics)*
  - ✔*PSPICE (OrCad)*
  - ✔*SABER (Analogy)*
  - ✔*SMARTSPICE (Silvaco)*
- Implementations in progress (autumn ‘98):
  - ✔*APLAC (Nokia, University of Helsinki)*
  - ✔*HSPICE/CMI (Avant!)*
  - ✔*SMASH (Dolphin Integration)*
  - ✔*SPECTRE (Cadence)*
  - ✔*SPICE3F5 (UC Berkeley)*
- ...check exact state of implementation with simulator vendors.

EKV v2.6 Model Parameters & Extraction Availability

- Extraction tools:
  - ✔*UTMOST (Silvaco)*
  - ✔*IC-CAP (HP),* custom parameter extraction through EPFL
- Support of EKV model parameters:
  - ✔*uEM Marin, Switzerland*
  - ✔*announced: MOSIS (US)/EUROPRACTICE (EU)*
  - ✔*evaluation in several European foundries*

EKV Model - Summary

- Need for a model dedicated to low-voltage, low-power analog and mixed analog-digital design and simulation
  - ✔*technology trends and scaling of supply voltage increase the importance of weak and moderate inversion regions*
- EKV v2.6: a model with unique features and capabilities:
  - ✔***first-order hand-calculation** possible!*
  - ✔***excellent weak and moderate inversion modelling***
  - ✔*major physical effects modelled, good adaptation to current CMOS technologies, acceptable results for deep sub-micron CMOS*
  - ✔***dedicated charge-based dynamic model** and **thermal noise model**; valid from weak to strong inversion, extensions for short-channel are being addressed*
  - ✔*uses only 18 intrinsic "core" parameters, simple parameter extraction method*
  - ✔***well suited for statistical circuit simulation including matching***

Outlook

☞ Current and future model developments include:

- ✔ *further refined mobility model*
- ✔ *weak inversion slope degradation for very short channel devices*
- ✔ *improved short-channel dynamic model*
- ✔ *polydepletion and quantum-mechanical effects*

☞ Current research in the context of the EKV MOSFET model:

- ✔ *RF modelling*
- ✔ *Low-temperature modelling*
- ✔ *Non-quasistatic modelling*
- ✔ *SOI modelling*

References

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