Design and tests of pixel readout circuits in 65 nm CMOS

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Motivation

- SVTs at the next generation colliders ask for highly pixellated detectors, with
  - analog (amplification, filtering, discrimination and possibly even A/D conversion)
  - digital (data sparsification, time stamping and buffering)
functions integrated in the pixel itself

- Designers are currently considering two different approaches:
  - moving to higher density 2D technology nodes
  - moving to 3D technologies with vertical integration techniques

- Standard 2D technologies: the 130 nm and 90 nm CMOS nodes are currently the focus of integrated circuit designers for the project of ASICs in future detector applications

- The 65 nm process is starting to be considered as a new attractive solution in view of the development of high-density, high-performance mixed-signal readout circuits

- Below 100 nm minimum feature size, the choice of the best technology to be used in ASIC design is a tricky problem, since transistor performance changes as CMOS technologies are scaled down into the nanoscale regime

- The impact of new dielectric materials and processing techniques (silicon strain, gate oxide nitridation) on the analog behavior of MOSFETs has to be carefully evaluated
Outline

• Analog performance of MOS transistors in the 65 nm node
  ○ Intrinsic Gain
  ○ Gate leakage current
  ○ Noise performance
    • White noise
    • 1/f noise
  ○ Radiation hardness

• Experimental results relevant to the Apsel65 prototype chip
  ○ Front-end channel features
  ○ Experimental results
    • Standalone channels
    • 3×3 Matrix
    • 8×8 Matrix
    • FFE Standalone channels
## Investigated Technologies

<table>
<thead>
<tr>
<th>65 nm Foundry A</th>
<th>90 nm Foundry A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Oxide Thickness</td>
<td>2.4 nm</td>
</tr>
<tr>
<td>Gate Capacitance</td>
<td>15 fF/μm²</td>
</tr>
<tr>
<td>Devices</td>
<td>Low Power</td>
</tr>
<tr>
<td>Layout</td>
<td>Open</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>90 nm Foundry B</td>
<td>90 nm Foundry B</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Oxide Thickness</td>
<td>2.6 nm</td>
</tr>
<tr>
<td>Gate Capacitance</td>
<td>13 fF/μm²</td>
</tr>
<tr>
<td>Devices</td>
<td>Low Power</td>
</tr>
<tr>
<td>Layout</td>
<td>Open</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>130 nm Foundry B</td>
<td>130 nm Foundry B</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Oxide Thickness</td>
<td>2.4 nm</td>
</tr>
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</tr>
<tr>
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<td>General Purp.</td>
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<tr>
<td>Layout</td>
<td>Open</td>
</tr>
</tbody>
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Intrinsic Gain

- It represents the maximum gain obtainable from a single transistor
  
  \[ \text{Intrinsic Gain} = \frac{g_m}{g_{ds}} \propto \alpha L \]

- \( g_m \) channel transconductance
- \( g_{ds} \) output conductance
- \( \alpha \) scaling factor

- Devices in the plot are biased at the same inversion level expressed by the Inversion Coefficient \( IC_0 = I_D/(I_Z^* W/L) \) where \( I_Z^* \) is the characteristic normalized drain current

- The intrinsic gain
  - is proportional to the channel length
  - is maintained across technology nodes (\( L_{\text{min}} \) scales by the same factor \( \alpha \))
• As a function of the **Inversion Coefficient**, the intrinsic gain:
  ー is independent of the drain current in weak inversion
  ー decreases with the drain current in strong inversion

• As a function of the **Channel Length**, the intrinsic gain:
  ー is proportional to the channel length for \( L \) close to \( L_{\text{min}} \) (DIBL dominates on \( g_{ds} \))
  ー shows a reduced slope for \( L > 5L_{\text{min}} \) (CLM effects dominate on \( g_{ds} \))
Gate Leakage Current

Gate current density:

\[ J_G = \frac{I_G}{(WL)} \]

- The current density may vary between 90 nm processes from two foundries.
- 65 nm MOSFETs are in the same region of current density values as 90 nm Foundry A and 130 nm Foundry B devices.
- This region is well below the commonly used limit of 1 A/cm².
- CMOS scaling beyond 100 nm does not necessarily lead to very leaky devices.
Noise in MOS Transistor

Noise in the drain current of a MOSFET can be represented through an equivalent noise voltage source in series with the device gate.

\[
S_e^2(f) = S_w^2 + S_{1/f}^2(f)
\]

- **S\(_w\) - white noise**
  - channel thermal noise (main contribution in the considered operating conditions)
  - \(S_{ch}^2 = \frac{4k_B T \Gamma}{g_m}\)
  - \(k_B\) Boltzmann’s constant
  - \(T\) absolute temperature
  - \(\Gamma\) channel thermal noise coefficient
  - contributions from parasitic resistances

- **S\(_{1/f}\) - 1/f noise**
  - technology dependent contribution
  - \(S_{1/f}^2(f) = \frac{k_f}{C_{ox} W L f^{\alpha_f}}\)
  - \(k_f\) 1/f noise parameter
  - \(C_{ox}\) oxide capacitance
  - \(W\) channel width
  - \(L\) channel length
  - \(\alpha_f\) 1/f noise slope-related coefficient

White and 1/f noise have been measured on test devices with different geometries and biased at different drain currents.
White noise

Evaluated in terms of the equivalent channel thermal noise resistance:

\[ R_{eq} = \frac{S^2_W}{4k_B T} = \alpha_w \frac{n\gamma}{g_m} \]

- \( \alpha_w \) excess noise coefficient
- \( n \) proportional to \( I_D(V_{GS}) \) subthreshold characteristic
- \( \gamma \) channel thermal noise coefficient

- \( \alpha_w \approx 1 \) for N and PMOS with \( L > 65 \) nm \( \Rightarrow \) no sizable short channel effects in the considered operating regions (for 65 nm devices \( \alpha_w \approx 1.3 \))
- Negligible contributions from parasitic resistances
Noise in different CMOS nodes

- NMOSFETs belonging to different CMOS nodes, with the minimum $L$ allowed by each process.
- Since the oxide thickness $t_{ox}$ and the minimum $L$ scale with the same coefficient, the NMOSFETs feature approximatively the same value of the gate capacitance $C_G = WLC_{ox}$.

- $1/f$ noise: devices exhibit a similar $1/f$ noise $\Rightarrow$ the value of the $K_f$ parameter changes little across different CMOS generations.
- White noise: devices are biased close to weak inversion $\Rightarrow$ white noise is not sizably affected by $L$ and CMOS node variations even at minimum gate lengths, as it appears in the high frequency portion of the spectra.
Ionizing radiation effects in sub-100 nm CMOS

Radiation induced positive charge is removed from thin gate oxides by tunneling (which also prevents the formation of interface states)

- Isolation oxides remain thick (order of 100 nm) also in nanoscale CMOS, and they are radiation soft
- In NMOS edge effects due to radiation-induced positive charge in the STI oxide generate sidewall leakage paths
- In an interdigitated device, this can be modeled considering that two lateral transistors for each finger are turned on
- The effect of these parasitic device on the noise and static characteristics must be carefully evaluated
Drain Current Static Characteristics

$I_D(V_{GS})$ before and after exposure to a 10 Mrad total dose of $\gamma$-rays

- A larger amount of lateral leakage takes place in 130 nm devices
- The smaller $I_{D,\text{lat}}$ of 65 nm devices suggests that the sensitivity to positive charge buildup in STI oxides is mitigated by the higher doping of the P-type body with respect to less scaled processes
Noise in NMOSFETs

- Moderate 1/f noise increase at low current density, due to the contribution of lateral parasitic devices
- At higher currents the degradation is almost negligible because the impact of the parasitic lateral devices on the overall drain current is much smaller
- No increase in the white noise region is detected
- In PMOS, very small increase in the low-frequency part of the noise voltage spectrum, even at low current density
Remarks on 65 nm node

- Static, signal, noise measurements and radiation tests have been performed on devices belonging to a 65 nm CMOS process
  - Intrinsic gain is not degraded by scaling
  - Gate leakage current is well below the limit of 1 A/cm²
  - Channel thermal noise behavior is consistent with equations valid in weak/moderate inversion
  - Flicker noise comparison with previous CMOS nodes shows that scaling to the 65 nm process does not affect 1/f noise performances significantly
  - Radiation hardness tests confirm the high degree of tolerance to ionizing radiation that appears to be typical of sub-100 nm technologies

- At the 65 nm node, low-noise analog design, according to the study of key analog parameters, appears to be still viable

- We designed a prototype chip with mixed-signal readout circuits in a 65 nm CMOS process manufactured by IBM ⇒ APSEL65
Apsel65: a prototype DNW MAPS in 65 nm

Main design features
- Chip Bias $V_{DD}$: 1.2 V
- PA input $W/L$: 28/0.25
- PA input $I_D$: 14 $\mu$A
- Power consumption: 20 $\mu$W

PL Simulation results
- Charge sensitivity: 725 mV/fC
- Peaking time ($Q_{inj}=800$ e$^-$): 300 ns
- Equivalent Noise Charge: 38 e$^-$
- Threshold Dispersion: 38 e$^-$
Chip description

- CHi Standalone channels
  - $C_{inj} = 30 \text{ fF}$
  - Detector simulating cap
    - $C_D = 250 \text{ fF (CH1)}$
    - $C_D = 350 \text{ fF (CH2)}$
    - $C_D = 450 \text{ fF (CH3)}$
  - DNW sensor not connected

- M1 3x3 matrix
  - 40 $\mu\text{m}$ pixel pitch
  - all analog outputs accessible
  - $C_{inj} = 30 \text{ fF for the central pixel}$
  - 360 $\mu\text{m}^2$ DNW electrode area

- M2 8x8 matrix
  - 40 $\mu\text{m}$ pixel pitch
  - row by row, 8 // digital readout
  - 360 $\mu\text{m}^2$ DNW electrode area

- FCi FFE channel
  - $C_{inj} = 10 \text{ fF}$
  - Detector simulating cap
    - $C_D = 50 \text{ fF (FC1)}$
    - $C_D = 100 \text{ fF (FC2)}$
    - $C_D = 150 \text{ fF (FC3)}$
    - $C_D = 100 \text{ fF (FC4)}$
      - enclosed layout PA input device
  - DNW sensor not connected
Cell Layout

- Area $40 \times 40 \ \mu m^2$
- DNW collecting electrode (orange)
  - area $360 \ \mu m^2$
  - capacitance $340 \ fF$ (estimated)
  - $99\%$ efficiency at $V_{Th}=400 \ e^-$
- In this prototype the digital section is kept to a minimum (latch, OR gate, tri-state buffer).
- It is planned to include sparsification and time-stamping logic at the pixel level in more advanced versions (room for this already available)
Standalone Channels

- **Peaking time** (at analog buffer output) is close to 530 ns for $Q_{inj}=800$ e$^-$ (simulation: $t_p=300$ ns at shaper out, $t_p=420$ ns at analog buffer out)
- **Recovery time** increases linearly with the signal amplitude ($C_2$ is discharged by a constant current)
- **Charge sensitivity** has an average value of about 830 mV/fC (725 mV/fC simulated)
Noise in Standalone Channels

- **Measurement**
  \[ ENC = 10.4 + 83e^{-}/pF \]

- **Simulation**
  \[ ENC = 10.4 + 75e^{-}/pF \]

- The ENC increases with the increase of the detector simulating capacitance
- Measured ENC is about 10% higher with respect to simulated values
3×3 Matrix

- **Peaking time** is close to 460 ns for $Q_{inj}=800 \text{ e}^-$
- **Recovery time** does not increase linearly with the signal amplitude (non-optimal polarization of the circuit)
- **Charge sensitivity** of 625 mV/fC was measured for the central pixel of the matrix
- **Noise**: ENC=67 e$^-$ for the central pixel and an average 54 e$^-$ for the other cells
8×8 matrix

Threshold scan results

- **Noise:** ENC=59 e− rms (38 e− rms simulated)
- **Threshold dispersion:** $\sigma(V_{Th}) = 59$ e− (38 e− rms simulated)
- **Non-optimal polarization of the circuit**
Fast Front-End Standalone Channels

Channels conceived for the readout of high resistivity pixels

- Peaking time is close to 42 ns for $Q_{inj}=16000 \ e^-$ (25 ns simulated)
- Charge sensitivity of about 18 mV/fC was measured (42 mV/fC simulated)
- Noise: ENC=165 $e^-$ rms (200 $e^-$ rms simulated)
Conclusions

- The 65 nm process is starting to be considered by designers for the development of readout ASICs at the next generation colliders
- Static, signal, noise measurements and radiation tests have been performed on devices belonging to a 65 nm CMOS process
- A test chip including DNW MAPS has been submitted in a 65 nm CMOS process provided by IBM
- Measurement results from this prototype circuit are encouraging and provide useful information for future submissions and larger chips
- At the 65 nm nodes, low-noise analog design will pose challenges but, according to the study of key analog parameters and the prototype chip measurement results, appears to be still viable