A 1.6 ppm/°C bandgap voltage reference for an extended operating temperature range

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Abstract: A new CMOS bandgap voltage reference (BGR) is proposed and simulated using Silterra 0.13 µm CMOS technology. The proposed BGR utilizes 3 curvature-corrected current generators that compensate for the output voltage variation in an extended temperature range. The proposed circuit generates an output voltage of 1.181 V with a variation of 380 µV from −50 °C to 150 °C.

Keywords: CMOS bandgap reference, current-control circuit

Classification: Integrated circuits

References

1 Introduction

The BGR circuit is an important building block of electronic devices, such as analog-to-digital converter and digital-to-analog converter. The voltage reference of the first-order BGR is obtained by adding the voltage across a p-n diode to the voltage that is proportional to the absolute temperature (PTAT) [1, 2, 3]. The nonlinear voltage across the p-n diode, which is explained in [4], causes the variation in voltage reference. The proposed circuits in [5, 6, 7, 8, 9, 10] have been proven to compensate for the nonlinear voltage, which give optimum output voltage at operating temperatures between $-50 \, ^\circ\mathrm{C}$ to $125 \, ^\circ\mathrm{C}$. However, with increased temperature to $125 \, ^\circ\mathrm{C}$, the circuit suffers from a huge output voltage variation because of uncontrolled nonlinear current generators. To avoid this problem, an improvement in nonlinear current generator is proposed, whereby the nonlinear current can be controlled and the reference voltage can be optimized for a wider operating temperature range.

2 Proposed design

The principal operation of the proposed BGR is shown in Fig. 1. The proposed curvature-compensation technique has three nonlinear voltages $V_{NL1}$, $V_{NL2}$, and $V_{NL3}$, which are added to the first-order BGR. The nonlinear voltage $V_{NL1}$ compensates for the voltage reference at $T_1$, whereas $V_{NL2}$ and $V_{NL3}$ are produced for curvature correction between $T_2$ to $T_3$. The nonlinear voltages $V_{NL2}$ and $V_{NL3}$ act like voltage pulses that control the voltage reference variation at all temperatures from $T_2$ to $T_3$. As a result, the output voltage reference $V_{REF}$ with low variation can be achieved within the large temperature range of $T_1$ to $T_3$.

![Concept of the proposed BGR.](image)

To realize the curvature-corrected BGR, $I_{NL1}$, $I_{NL2}$, and $I_{NL3}$ generators, along with the first-order BGR and a startup circuit, are proposed and illustrated in Fig. 2. The output voltage $V_{REF0}$ of the first-order BGR is expressed as

$$V_{REF0} = \frac{R_3 + R_4}{R_1} V_T \ln(n) + V_{EB3}. \quad (1)$$

The nonlinear terms in $V_{EB3}$ [4], which cause output voltage variation at low and high temperatures, significantly vary from the reference voltage at typical temperatures.
The proposed $I_{NL1}$ generator $G_A$ fixes the voltage variation at a low temperature. The current $I_{PTAT}$ through the resistor $R_4$ produces a PTAT voltage given as

$$V_{G,MP6} = R_4 I_{PTAT},$$

where

$$I_{PTAT} = \frac{V_T \ln(n)}{R_1}.$$  

At a low temperature, $M_{P6}$ operates in saturation region, sourcing $I_{NL1}$ into the first-order BGR. The voltage change at the source terminal of $M_{P6}$ and $M_{P7}$ is reduced by setting the size of $M_{P7}$ to be larger than $M_{P6}$, which is detailed in [8]. With increased temperature, the gate voltage of $M_{P6}$ increases causing the decrease of the drain current, abruptly causing the transistor to move to cut-off region.

The second current generator $G_B$ operates in the opposite condition as compared to $G_A$. Initially at a temperature below $T_2$, the PTAT current will result in the voltage drop across $R_5$ such that $M_{P9}$ is in the cut-off region. Hence, $I_{NL2}$ exhibits negligible current. However, beyond $T_2$, the PTAT current flows through $M_{P6}$, which is mirrored to $R_5$. A PTAT voltage given as

$$V_{G,MP9} = R_5 I_{PTAT}$$

drives $M_{P9}$ in saturation region, thereby producing significant nonlinear current $I_{NL2}$. The operation is similar in current generator $G_C$, where $I_{NL3}$ is produced and added to the first-order BGR. $M_{N3}$ and $R_6$ limit $I_{NL2}$ to a certain amount and pull the current down with increased temperature, whereas $M_{N6}$ and $R_8$ control $I_{NL3}$ at a higher temperature. $M_{P9}$ and $M_{P11}$ set the amount of current $I_{NL2}$ and $I_{NL3}$, respectively. $R_6$ is set to be larger than $R_8$. By increasing the temperature, $M_{N3}$ is cut-off earlier than $M_{N6}$.

The output voltage reference of the proposed circuit is given by

$$V_{REF} = \frac{R_2 + R_3}{R_1} V_T \ln(n) + V_{EB3} + (I_{NL1} + I_{NL2} + I_{NL3}) R_3,$$
where \( n \) is the emitter-area ratio of \( Q_1 \) and \( Q_2 \), and \( I_{NL1}, I_{NL2}, \) and \( I_{NL3} \) are nonlinear currents flowing through \( MP_6, MP_9 \) and \( MP_{11} \), respectively.

### 3 Simulation results and discussions

The proposed BGR shown in Fig. 2 is simulated with Silterra 0.13 \( \mu \)m process. The simulated voltage references and nonlinear current are plotted in Fig. 3. The maximum currents of 300, 150, and 400 nA are obtained for \( I_{NL1}, I_{NL2}, \) and \( I_{NL3} \), respectively. The reference voltage is proportionally grown to the nonlinear current plotted at \(-50, 105, \) and \(135^\circ \text{C} \). The maximum and minimum output voltages of the proposed BGR are 1.18102 and 1.18140 V respectively. Hence, the temperature coefficient of 1.6 ppm/\( ^\circ \text{C} \) is obtained within the temperature range of \(-50^\circ \text{C} \) to \(150^\circ \text{C} \), which is fivefold smaller than the temperature coefficient achieved from the first-order BGR.

Table I compares the performance of the proposed curvature-compensated BGR circuits with that of [7] and [9]. The proposed BGR’s temperature coefficient of 1.6 ppm/\( ^\circ \text{C} \) is better than the other designs. The simulation results under the influence of the 3 current generators indicate that the

![Proposed curvature-corrected BGR circuit.](image)

**Table I.** Comparison of the proposed curvature-compensated BGR with previous work

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[7]</th>
<th>[9]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Year Reported</td>
<td>2003</td>
<td>2009</td>
<td>2014</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>2.0–4.0</td>
<td>1.7–4.0</td>
<td>2.5</td>
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<tr>
<td>Current Cons. (µA)</td>
<td>23 (max.)</td>
<td>12–28</td>
<td>36</td>
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<tr>
<td>Ref. Voltage (V)</td>
<td>1.14205</td>
<td>1.317</td>
<td>1.181</td>
</tr>
<tr>
<td>Temp. Range (°C)</td>
<td>0 to 100</td>
<td>10 to 125</td>
<td>-50 to 150</td>
</tr>
<tr>
<td>TC (ppm/°C)</td>
<td>2.6–6.1</td>
<td>10</td>
<td>1.6</td>
</tr>
<tr>
<td>CMOS Technology</td>
<td>0.6-µm</td>
<td>0.5-µm</td>
<td>0.13-µm</td>
</tr>
</tbody>
</table>
The proposed curvature-compensation technique can be used to improve the TC of the BGR. More notably, with the addition of the third current generator \( G_C \), the temperature range is extended to 150 °C. Hence, the uncontrolled voltage variation beyond 125 °C can be alleviated.

## 4 Conclusion

A CMOS bandgap voltage reference with the new curvature-corrected technique is proposed. Based on this technique, the output voltage reference of 1.181 V with 380 \( \mu \)V variation is obtained, operating within the extended temperature range of \(-50°\)C to 150 °C. The circuit is designed to operate at 2.5 V supply voltage. The accuracy of the proposed BGR is fivefold higher than that of the first-order BGR.

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